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TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC4051BP, TC4051BF, TC4051BFT TC4052BP, TC4052BF, TC4052BFT TC4053BP, TC4053BF, TC4053BFT

TC4051B

Single 8-Channel Multiplexer/Demultiplexer

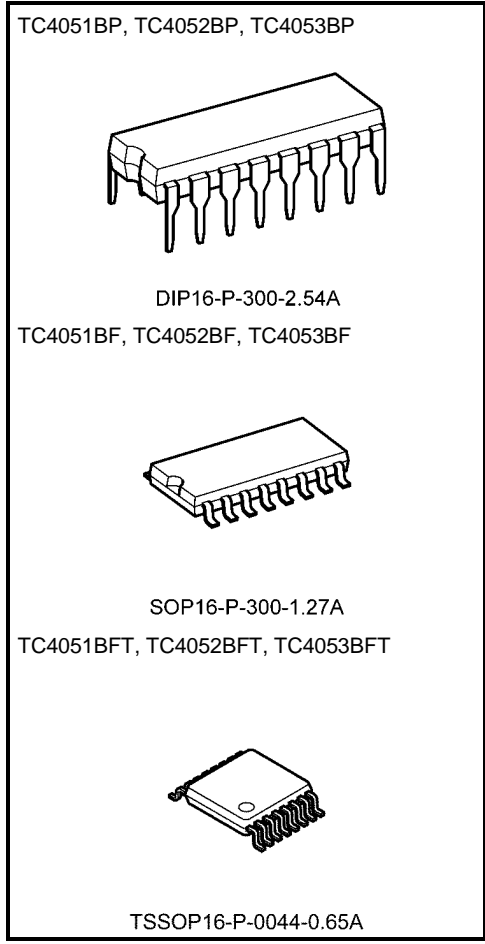
TC4052B

Differential 4-Channel  
 Multiplexer/Demultiplexer

TC4053B

Triple 2-Channel Multiplexer/Demultiplexer

TC4051B, TC4052B and TC4053B are multiplexers with capabilities of selection and mixture of analog signal and digital signal. TC4051B has 8 channels configuration. TC4052B has 4 channel × 2 configuration and TC4053B has 2 channel × 3 configuration. The digital signal to the control terminal turns "ON" the corresponding switch of each channel, with large amplitude ( $V_{DD} - V_{EE}$ ) can be switched by the control signal with small logical amplitude ( $V_{DD} - V_{SS}$ ). For example, in the case of  $V_{DD} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$  and  $V_{EE} = -5\text{ V}$ , signals between  $-5\text{ V}$  and  $+5\text{ V}$  can be switched from the logical circuit with single power supply of 5 volts. As the ON-resistance of each switch is low, these can be connected to the circuits with low input impedance.

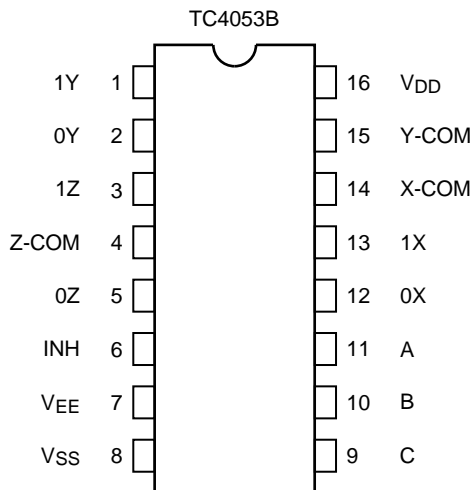
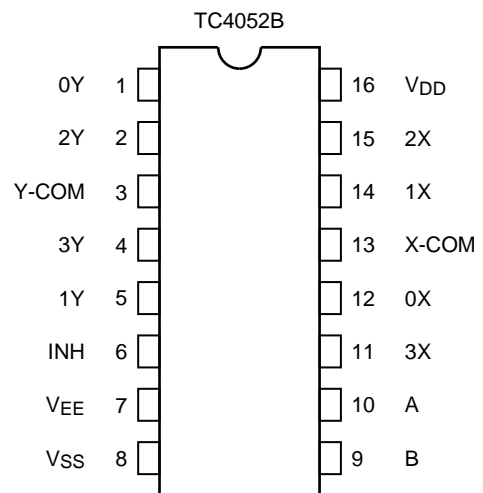
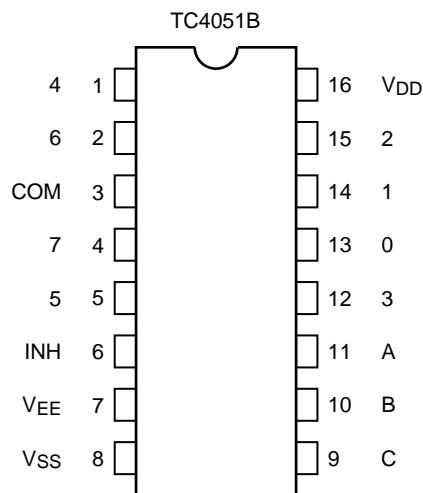


Weight

DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
TSSOP16-P-0044-0.65A	: 0.06 g (typ.)

Start of commercial production  
 1978-04

## Pin Assignment (top view)



## Truth Table

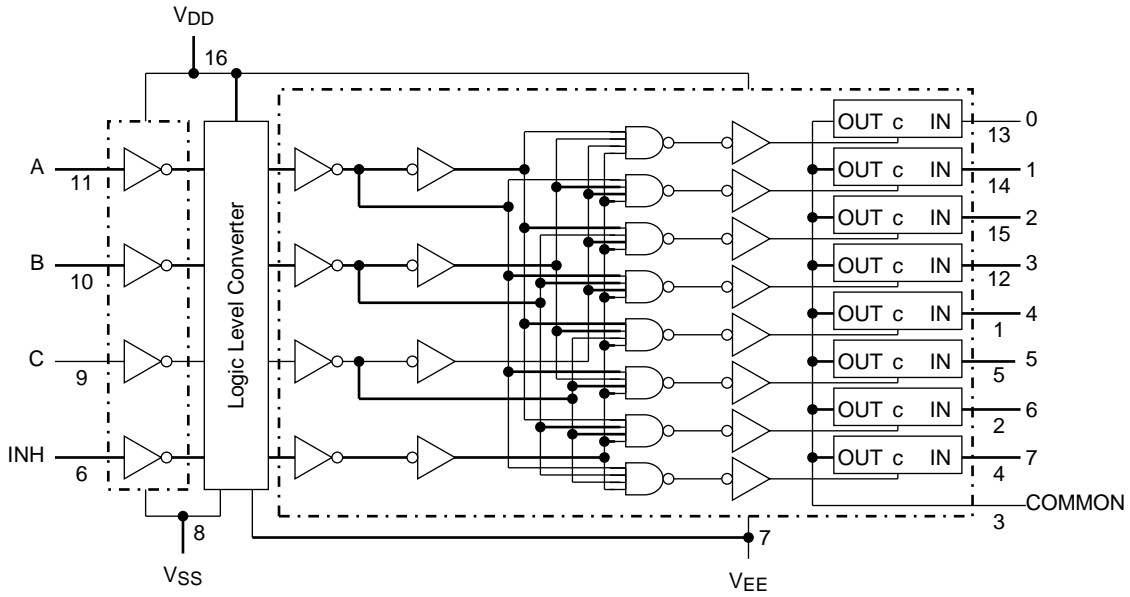
Control Inputs				"ON" Channel		
Inhibit	C $\Delta$	B	A	TC4051B	TC4052B	TC4053B
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z
L	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	L	L	4	—	0X, 0Y, 1Z
L	H	L	H	5	—	1X, 0Y, 1Z
L	H	H	L	6	—	0X, 1Y, 1Z
L	H	H	H	7	—	1X, 1Y, 1Z
H	X	X	X	None	None	None

X: Don't care

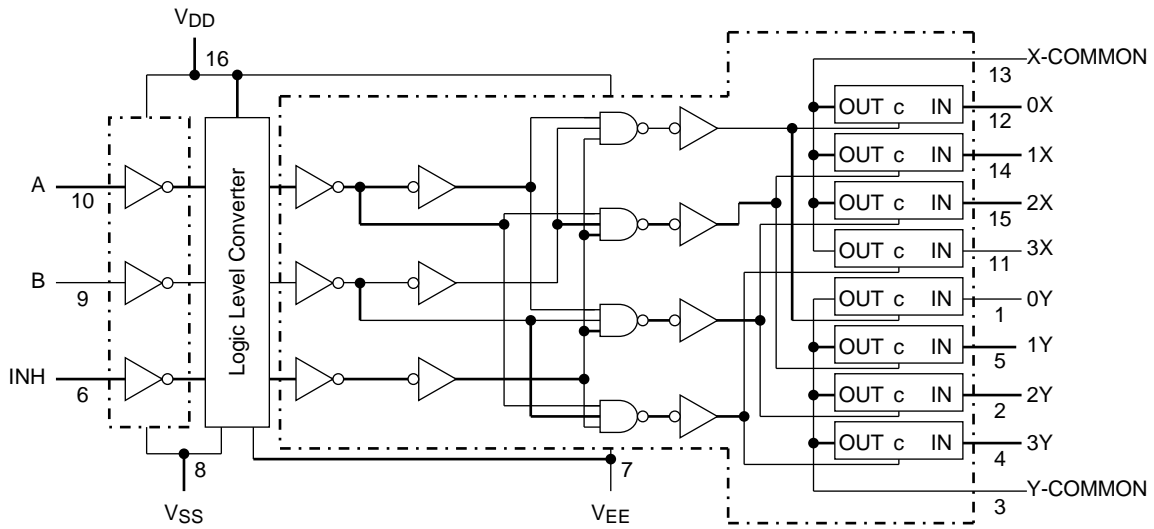
$\Delta$ : Except TC4052B

**Logic Diagram**

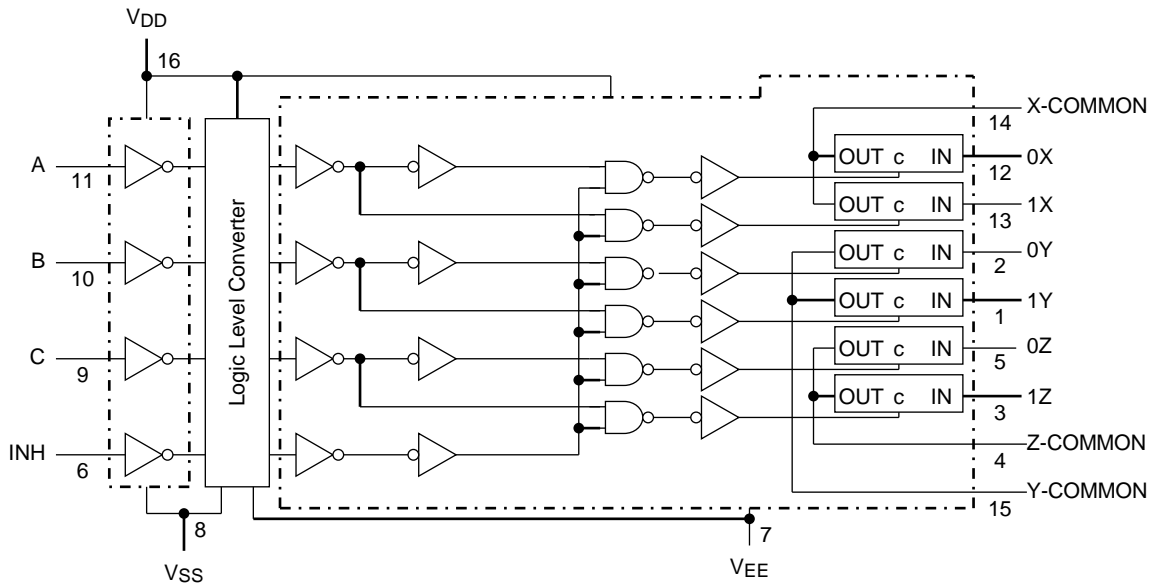
**TC4051B**



**TC4052B**



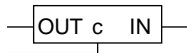
## TC4053B



### Truth Table

Control C	Impedance between IN-OUT (Note)
H	$0.5 \text{ to } 5 \times 10^2 \Omega$
L	$>10^9 \Omega$

Note: See electrical characteristics



### Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	$V_{DD}-V_{SS}$	-0.5 to 20	V
DC supply voltage	$V_{DD}-V_{EE}$	-0.5 to 20	V
Control input voltage	$V_{CIN}$	$V_{SS} - 0.5 \text{ to } V_{DD} + 0.5$	V
Switch I/O voltage	$V_I/V_O$	$V_{EE} - 0.5 \text{ to } V_{DD} + 0.5$	V
Control input current	$I_{CIN}$	$\pm 10$	mA
Potential difference across I/O during ON	$V_I-V_O$	-0.5 to 0.5	V
Power dissipation	$P_D$	300 (DIP)/180 (SOP/TSSOP)	mW
Operating temperature range	$T_{opr}$	-40 to 85	$^{\circ}\text{C}$
Storage temperature range	$T_{stg}$	-65 to 150	$^{\circ}\text{C}$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
DC supply voltage	VDD-VSS	—	3	—	18	V
	VDD-VEE	—	3	—	18	
Control input voltage	V <sub>IN</sub>	—	V <sub>SS</sub>	—	V <sub>DD</sub>	V
Input/output voltage	V <sub>IN</sub> /V <sub>OUT</sub>	—	V <sub>EE</sub>	—	V <sub>DD</sub>	V

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused Control inputs must be tied to either V<sub>DD</sub> or V<sub>SS</sub>.

## Static Electrical Characteristics

Characteristics	Symbol	Test Condition	-40°C			25°C			85°C		Unit			
			V <sub>SS</sub> (V)	V <sub>EE</sub> (V)	V <sub>DD</sub> (V)	Min	Max	Min	Typ.	Max		Min	Max	
Control input high voltage	V <sub>IH</sub>	V <sub>IS</sub> = V <sub>DD</sub> thru 1 kΩ	V <sub>EE</sub> = V <sub>SS</sub> R <sub>L</sub> = 1 kΩ to V <sub>SS</sub>	5	3.5	—	3.5	2.75	—	3.5	—	V		
				10	7.0	—	7.0	5.50	—	7.0	—			
				15	11.0	—	11.0	8.25	—	11.0	—			
Control input low voltage	V <sub>IL</sub>			I <sub>IS</sub> < 2 μA on all OFF channels	5	—	1.5	—	2.25	1.5	—	1.5	V	
					10	—	3.0	—	4.5	3.0	—	3.0		
					15	—	4.0	—	6.75	4.0	—	4.0		
On-state resistance	R <sub>ON</sub>	0 ≤ V <sub>IS</sub> ≤ V <sub>DD</sub> R <sub>L</sub> = 10 kΩ	0		0	5	—	850	—	240	950	—	1200	Ω
			0		0	10	—	210	—	110	250	—	300	
			0		0	15	—	140	—	80	160	—	200	
ΔOn-state resistance between any 2 switches	R <sub>ONΔ</sub>		—	0	0	5	—	—	—	10	—	—	—	Ω
				0	0	10	—	—	—	6	—	—	—	
				0	0	15	—	—	—	4	—	—	—	
Input/output leakage current	I <sub>OFF</sub>	V <sub>IN</sub> = 18 V, V <sub>OUT</sub> = 0 V V <sub>IN</sub> = 0 V, V <sub>OUT</sub> = 18 V		18	—	±100	—	±0.01	±100	—	±1000	nA		
				18	—	±100	—	±0.01	±100	—	±1000			
Quiescent supply current	I <sub>DD</sub>	V <sub>IN</sub> = V <sub>SS</sub> , V <sub>DD</sub>		(Note)	5	—	5.0	—	0.005	5.0	—	150	μA	
			10		—	10	—	0.010	10	—	300			
			15		—	20	—	0.015	20	—	600			
Input current	I <sub>IN</sub>	V <sub>IH</sub> = 18 V V <sub>IL</sub> = 0 V	18	—	0.1	—	10 <sup>-5</sup>	0.1	—	1.0	μA			
			18	—	-0.1	—	-10 <sup>-5</sup>	-0.1	—	-1.0				
Input capacitance	C <sub>IN</sub>	—	—	—	—	—	—	5	7.5	—	—	pF		
Switch input capacitance	C <sub>IN</sub>	—	—	—	—	—	—	10	—	—	—	pF		
Output capacitance	C <sub>OUT</sub>	TC4051B	10	—	—	—	—	58	—	—	—	pF		
		TC4052B	10	—	—	—	—	30	—	—	—			
		TC4053B	10	—	—	—	—	17	—	—	—			
Feedthrough capacitance	C <sub>IN</sub> - C-OUT	TC4051B	10	—	—	—	—	0.2	—	—	—	pF		
		TC4052B	10	—	—	—	—	0.2	—	—	—			
		TC4053B	10	—	—	—	—	0.2	—	—	—			

Note: All valid input combinations.

## Switching Characteristics (Ta = 25°C, CL = 50 pF)

Characteristics	Symbol	Test Condition			Min	Typ.	Max	Unit		
		VSS (V)	VEE (V)	VDD (V)						
Phase difference between input to output	φI-O	—	0	0	5	—	15	45	ns	
			0	0	10	—	8	20		
			0	0	15	—	6	15		
Propagation delay time (A, B, C, -OUT)	tpZL tpZH tpLZ tpHZ	RL = 1 kΩ	0	0	5	—	170	550	ns	
			0	0	10	—	90	240		
			0	0	15	—	70	160		
			0	-5	5	—	100	240		
			0	-7.5	7.5	—	80	160		
Propagation delay time (INH-OUT)	tpZL tpZH	RL = 1 kΩ	0	0	5	—	120	380	ns	
			0	0	10	—	60	200		
			0	0	15	—	50	160		
			0	-5	5	—	80	200		
			0	-7.5	7.5	—	60	160		
Propagation delay time (INH-OUT)	tpLZ tpHZ	RL = 1 kΩ	0	0	5	—	170	450	ns	
			0	0	10	—	90	210		
			0	0	15	—	70	160		
			0	-5	5	—	100	210		
			0	-7.5	7.5	—	80	160		
-3dB cutoff frequency TC4051B TC4052B TC4053B	fmax (I-O)	RL = 1 kΩ	(Note 1)	-5	-5	5	—	20	—	MHz
				-5	-5	5	—	30	—	
				-5	-5	5	—	40	—	
Total harmonic distortion	—	RL = 10 kΩ f = 1 kHz	(Note 2)	-2.5	-2.5	2.5	—	0.15	—	%
				-5	-5	5	—	0.03	—	
				-7.5	-7.5	7.5	—	0.02	—	
-50dB feedthrough (switch off)	—	RL = 1 kΩ	(Note 3)	-5	-5	5	—	500	—	kHz
Crosstalk	—	RL = 1 kΩ	(Note 4)	-5	-5	5	—	1.5	—	MHz
Crosstalk (control-OUT)	—	RLIN = 1 kΩ		0	0	5	—	200	—	mV
		ROUT = 10 kΩ		0	0	10	—	400	—	
		CL = 15 pF		0	0	15	—	600	—	

Note 1: Sine wave of  $\pm 2.5$  Vp-p shall be used for Vis and the frequency of  $20 \log_{10} \frac{V_{OS}}{V_{is}} = -3\text{dB}$  shall be fmax.

Note 2: Vis shall be sine wave of  $\pm \left( \frac{V_{DD} - V_{EE}}{4} \right)$  p-p.

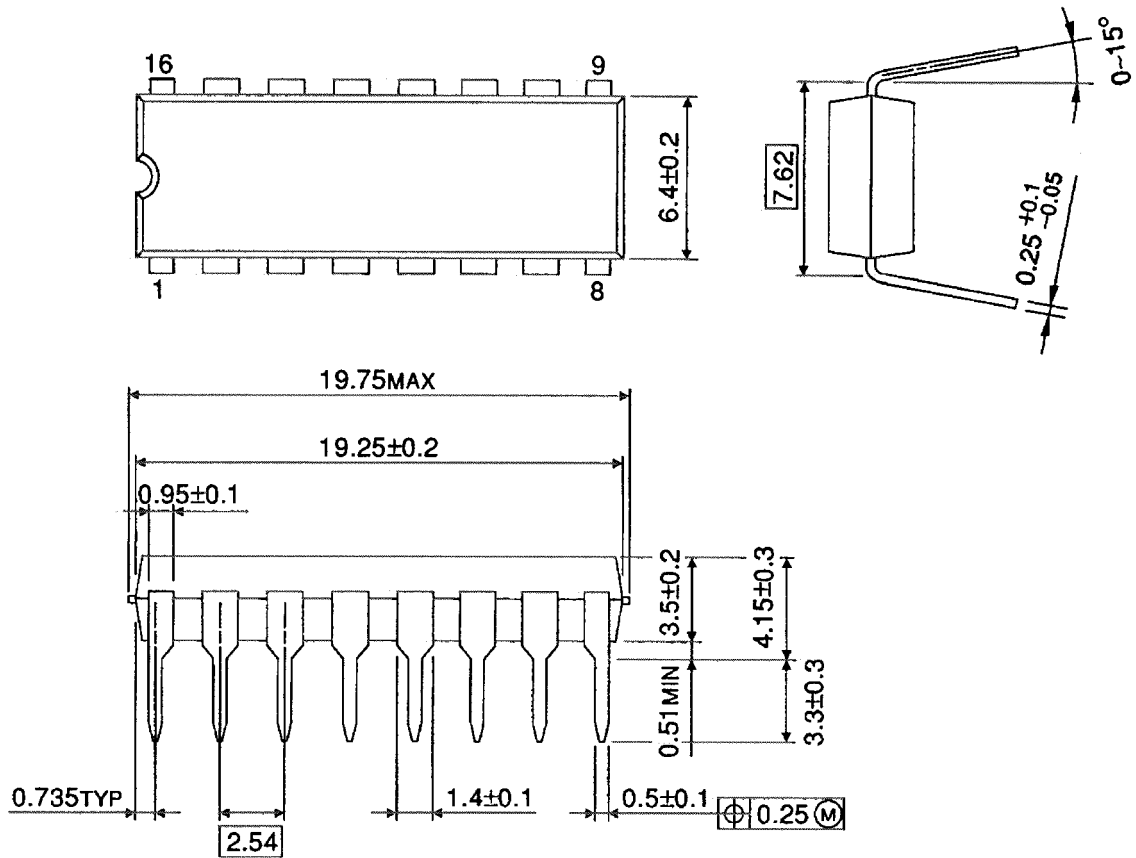
Note 3: Sine wave of  $\pm 2.5$  Vp-p shall be used for Vis and the frequency of  $20 \log_{10} \frac{V_{OS}}{V_{is}} = -50\text{dB}$  shall be feed-through.

Note 4: Sine wave of  $\pm 2.5$  Vp-p shall be used for Vis and the frequency of  $20 \log_{10} \frac{V_{OS}}{V_{is}} = -50\text{dB}$  shall be crosstalk.

## Package Dimensions

DIP16-P-300-2.54A

Unit : mm



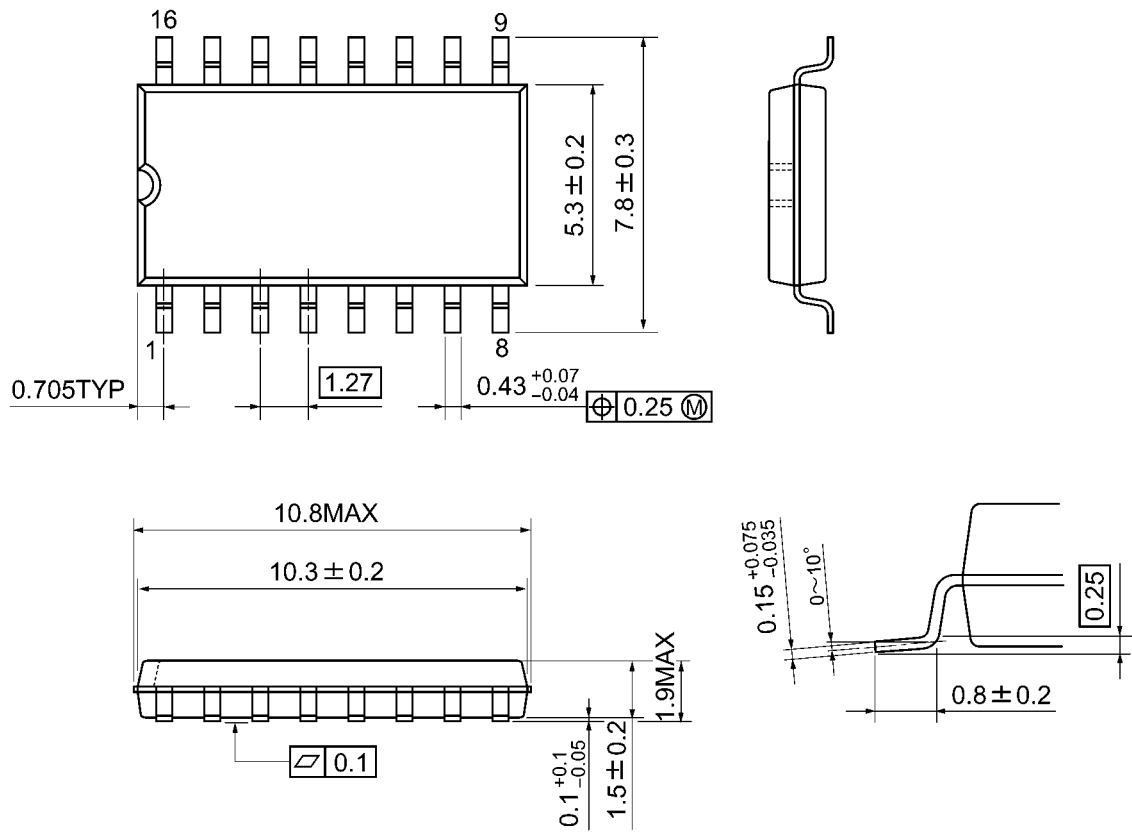
Weight: 1.00 g (typ.)



## Package Dimensions

SOP16-P-300-1.27A

Unit: mm

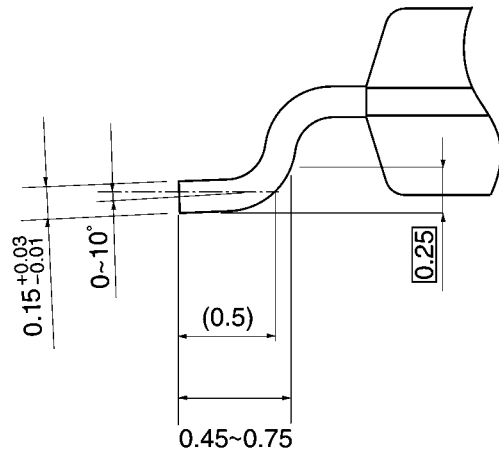
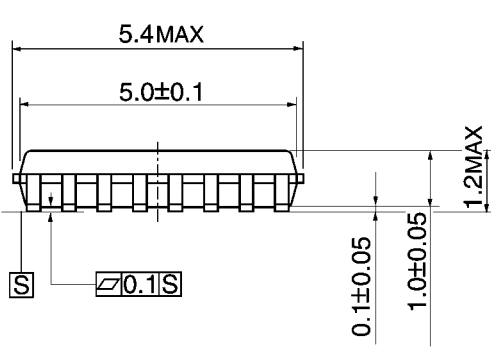
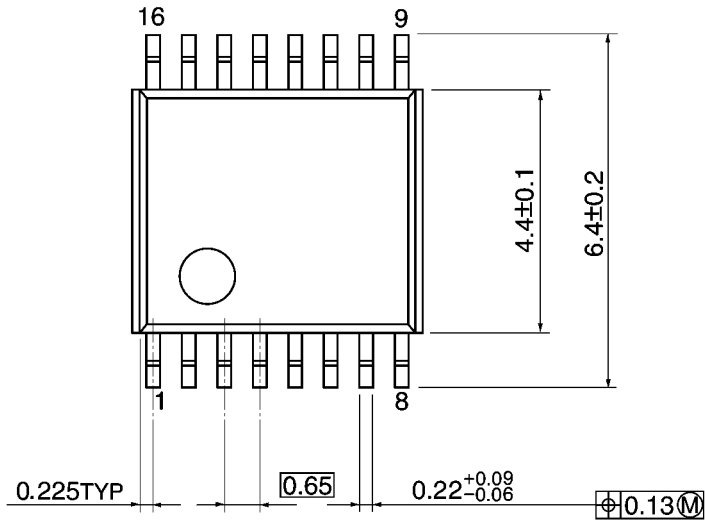


Weight: 0.18 g (typ.)

## Package Dimensions

TSSOP16-P-0044-0.65A

Unit: mm



Weight: 0.06 g (typ.)

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