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December 2003

LF353
Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

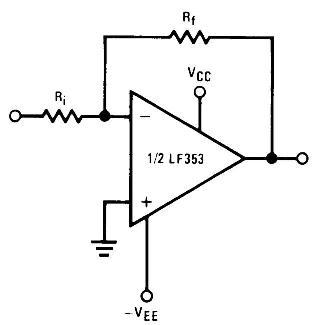
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

- Internally trimmed offset voltage: 10 mV
- Low input bias current: 50pA
- Low input noise voltage: 25 nV/√Hz
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/µs
- Low supply current: 3.6 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion : ≤0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 µs

Typical Connection



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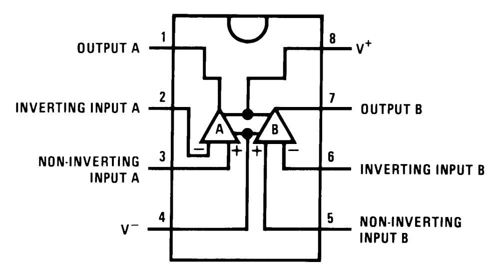
Connection Diagram

Dual-In-Line Package



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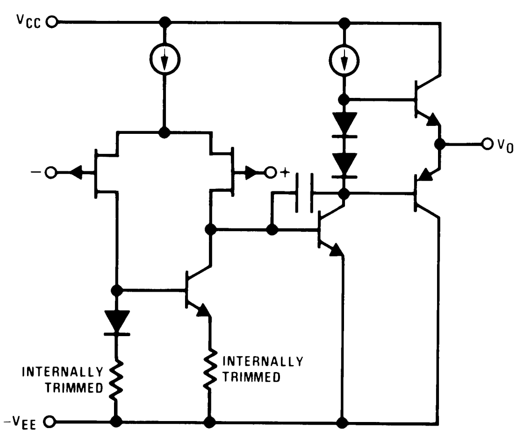
Top View
Order Number LF353M, LF353MX or LF353N
See NS Package Number M08A or N08E

Simplified Schematic

1/2 Dual



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BI-FET II™ is a trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 2)
Operating Temperature Range	0˚C to +70˚C
T_j(MAX)	150˚C
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65˚C to +150˚C
Lead Temp. (Soldering, 10 sec.)	260˚C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260˚C
Small Outline Package	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 8)	1000V
θ_{JA} M Package	TBD

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

DC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			MIn	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10kΩ, T_A=25˚C		5	10	mV
		Over Temperature			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10		µV/˚C
I_{OS}	Input Offset Current	T_j=25˚C, (Notes 5, 6)		25	100	pA
		T_j≤70˚C			4	nA
I_B	Input Bias Current	T_j=25˚C, (Notes 5, 6)		50	200	pA
		T_j≤70˚C			8	nA
R_{IN}	Input Resistance	T_j=25˚C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25˚C	25	100		V/mV
		V_O=±10V, R_L=2 kΩ				
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage	V_S=±15V	±11	+15		V
	Range			−12		V
CMRR	Common-Mode Rejection Ratio	R_S≤ 10kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	70	100		dB
I_S	Supply Current			3.6	6.5	mA

AC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25˚C, f=1 Hz−20 kHz		−120		dB
		(Input Referred)				
SR	Slew Rate	V_S=±15V, T_A=25˚C	8.0	13		V/µs
GBW	Gain Bandwidth Product	V_S=±15V, T_A=25˚C	2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25˚C, R_S=100Ω, f=1000 Hz		16		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j=25˚C, f=1000 Hz		0.01		$pA/\sqrt{Hz}$

AC Electrical Characteristics (Continued)

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
THD	Total Harmonic Distortion	A_V=+10, RL=10k, V_O=20Vp–p, BW=20 Hz-20 kHz		<0.02		%

Note 2: For operating at elevated temperatures, the device must be derated based on a thermal resistance of 115˚C/W typ junction to ambient for the N package, and 158˚C/W typ junction to ambient for the H package.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: The power dissipation limit, however, cannot be exceeded.

Note 5: These specifications apply for V_S=±15V and 0˚C≤T_A≤+70˚C. V_{OS}, $I_B$and I_{OS} are measured at V_{CM}=0.

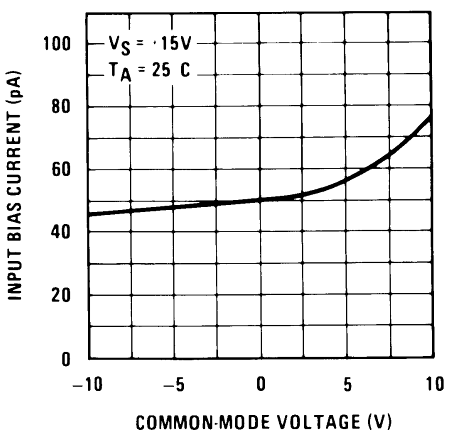
Note 6: The input bias currents are junction leakage currents which approximately double for every 10˚C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j=T_A+θ_{jA} P_D where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

Input Bias Current



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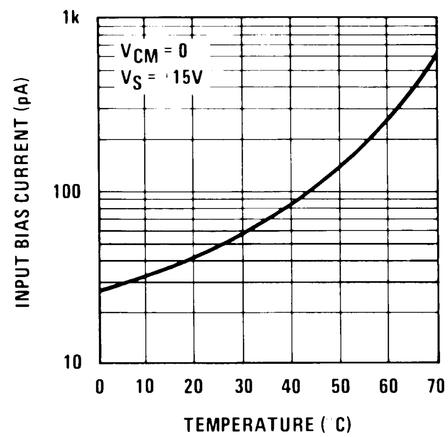
Input Bias Current



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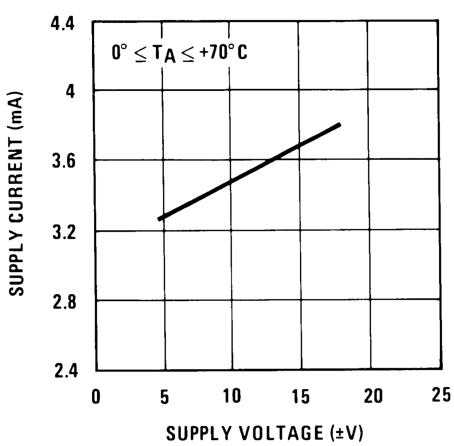
Supply Current



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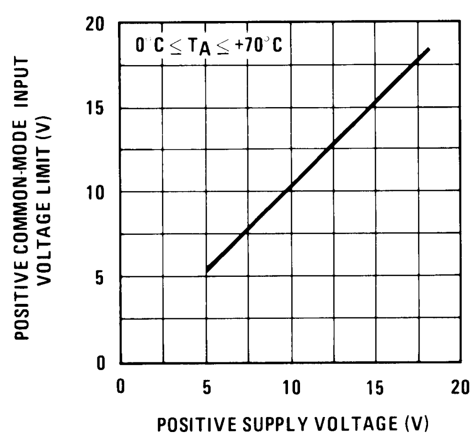
Positive Common-Mode Input Voltage Limit



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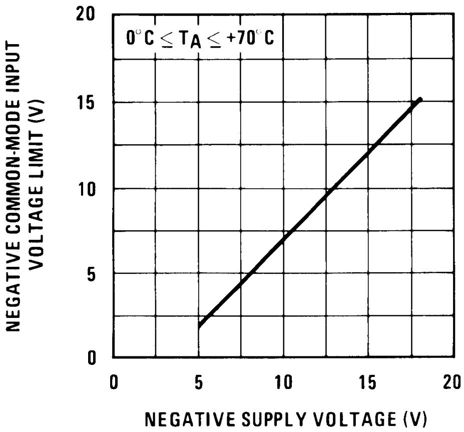
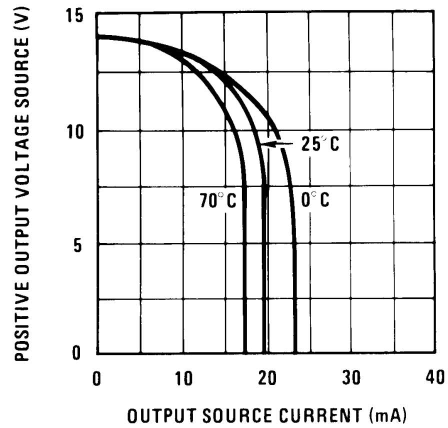
Typical Performance Characteristics (Continued)

Negative Common-Mode Input Voltage Limit



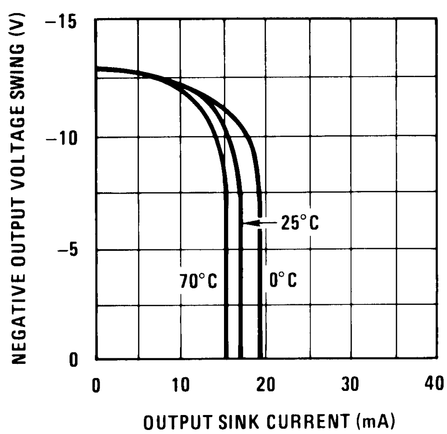
00564922

Positive Current Limit



00564923

Negative Current Limit



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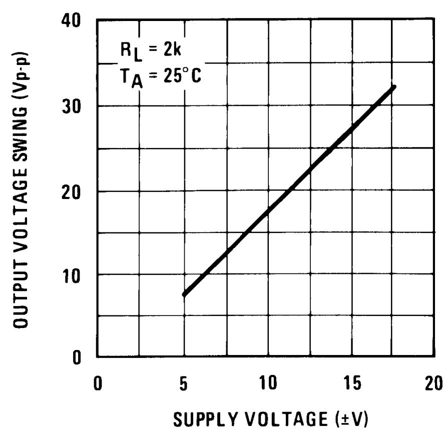
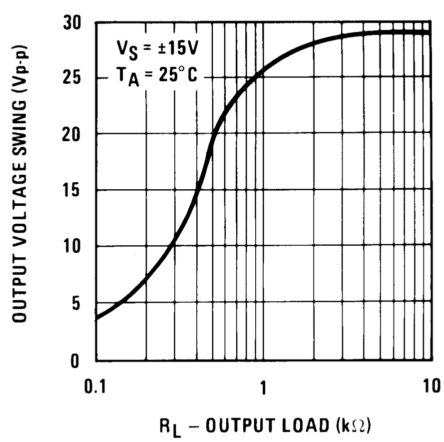
Voltage Swing



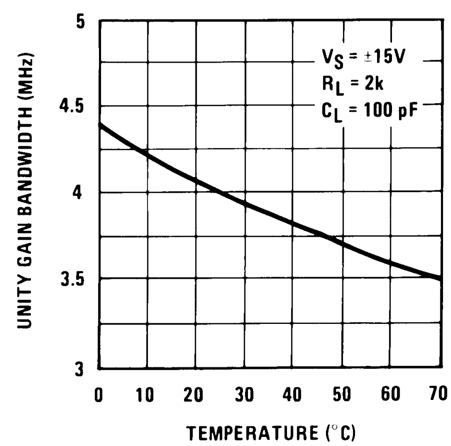
00564925

Output Voltage Swing



00564926

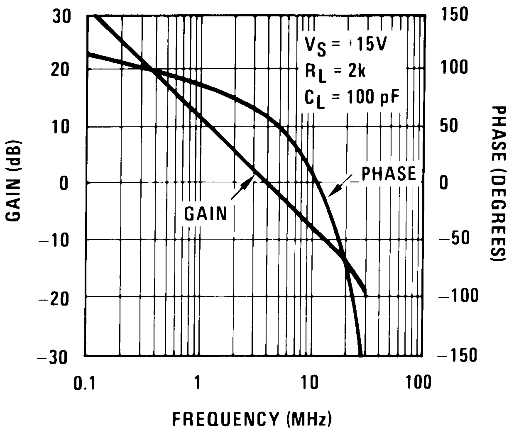
Gain Bandwidth



00564927

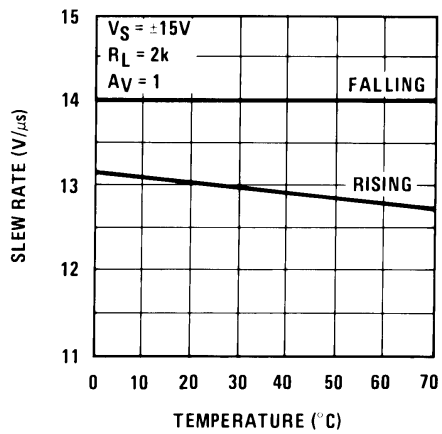
Typical Performance Characteristics (Continued)

Bode Plot



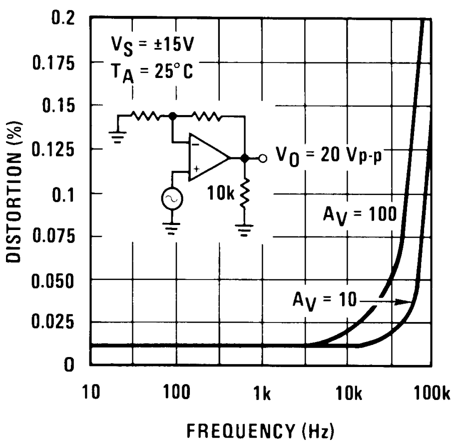
00564928

Slew Rate



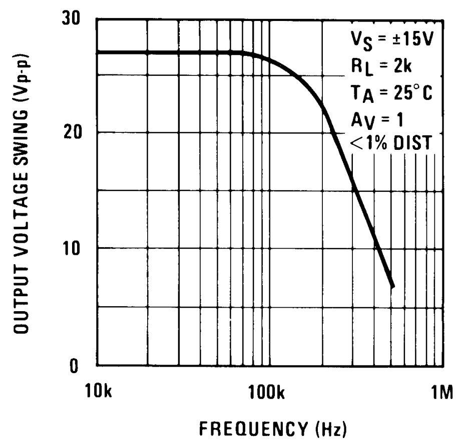
00564929

Distortion vs. Frequency



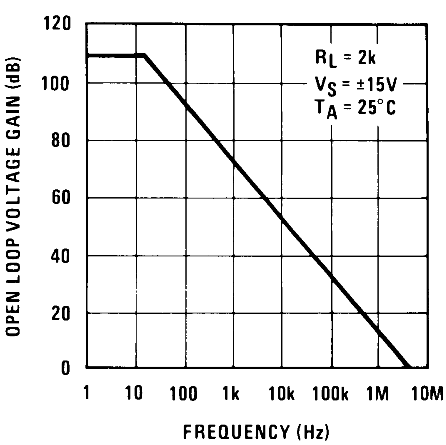
00564930

Undistorted Output Voltage Swing



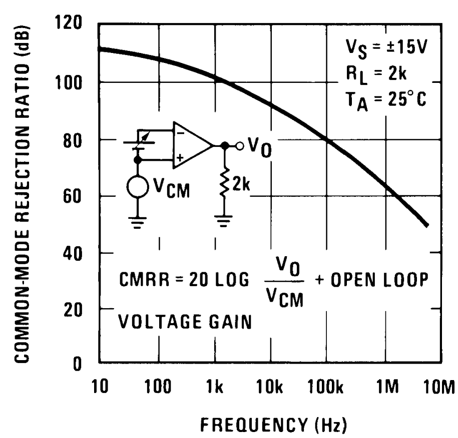
00564931

Open Loop Frequency Response



00564932

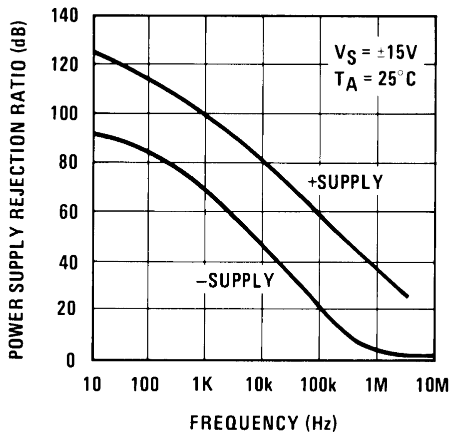
Common-Mode Rejection Ratio



00564933

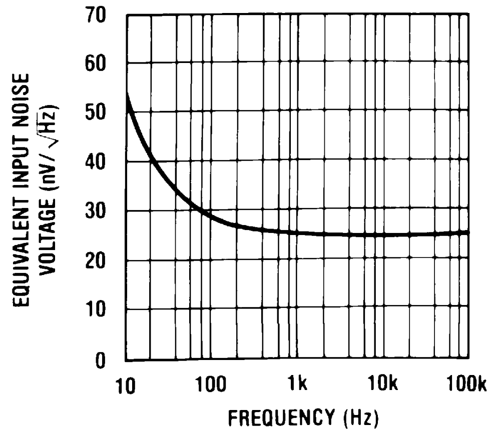
Typical Performance Characteristics (Continued)

Power Supply Rejection Ratio



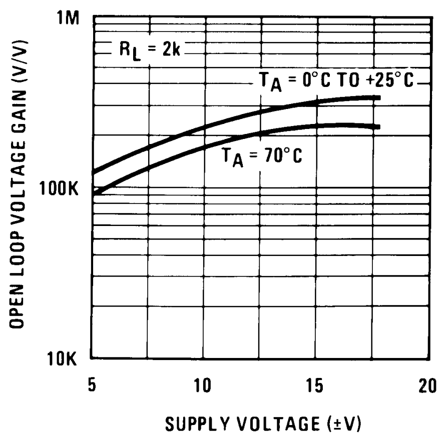
00564934

Equivalent Input Noise Voltage



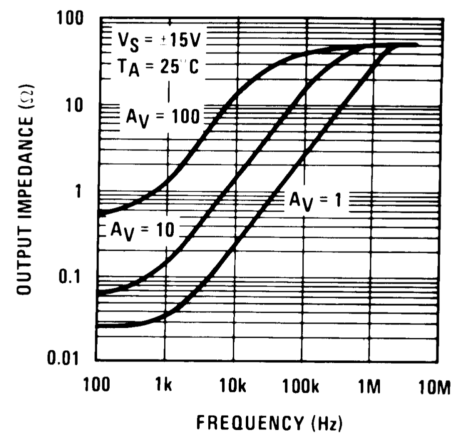
00564935

Open Loop Voltage Gain (V/V)



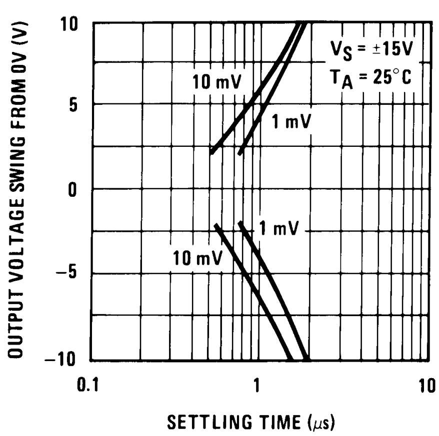
00564936

Output Impedance



00564937

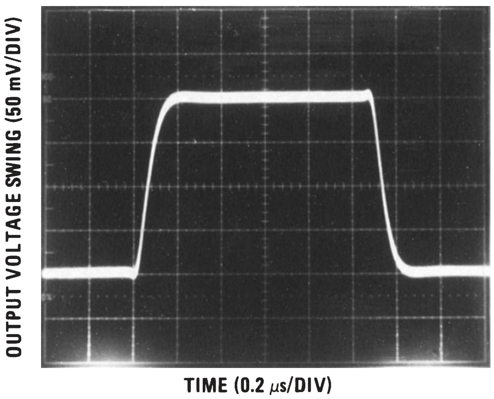
Inverter Settling Time



00564938

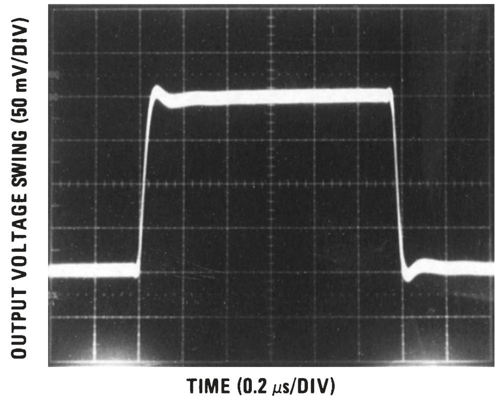
Pulse Response

Small Signaling Inverting



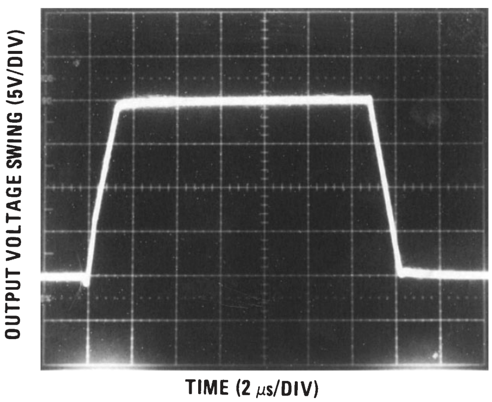
00564904

Small Signal Non-Inverting



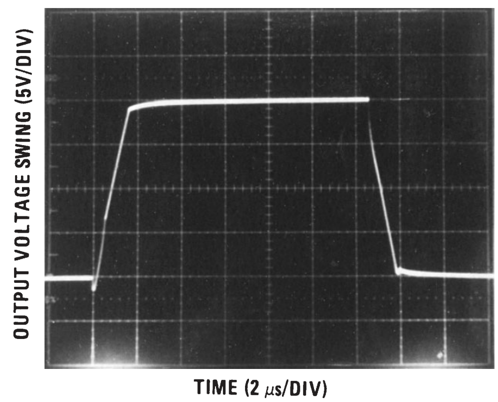
00564905

Large Signal Inverting



00564906

Large Signal Non-Inverting



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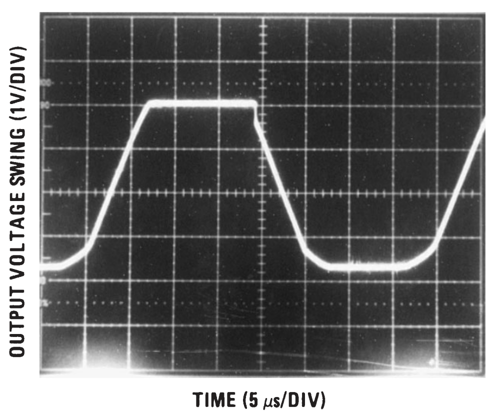
Current Limit (R_L = 100Ω)



00564908

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur

Application Hints (Continued)

since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

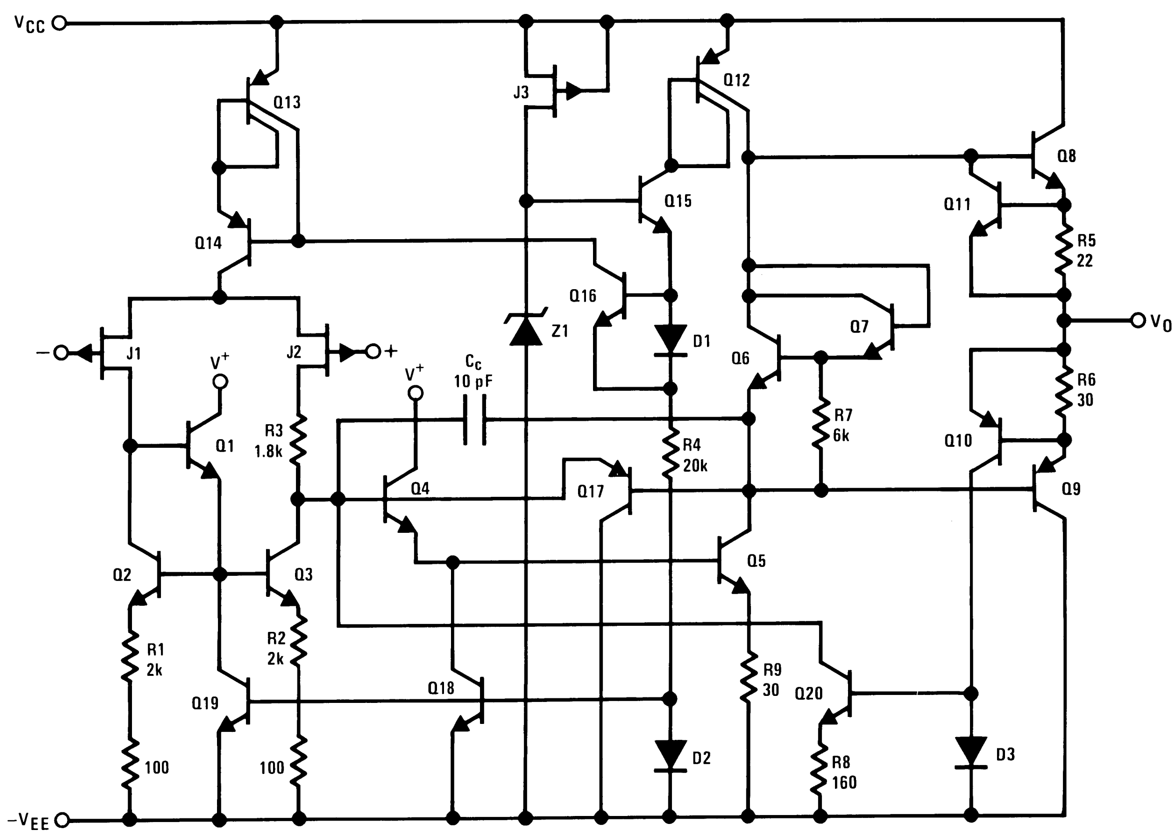
The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0˚C to +70˚C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

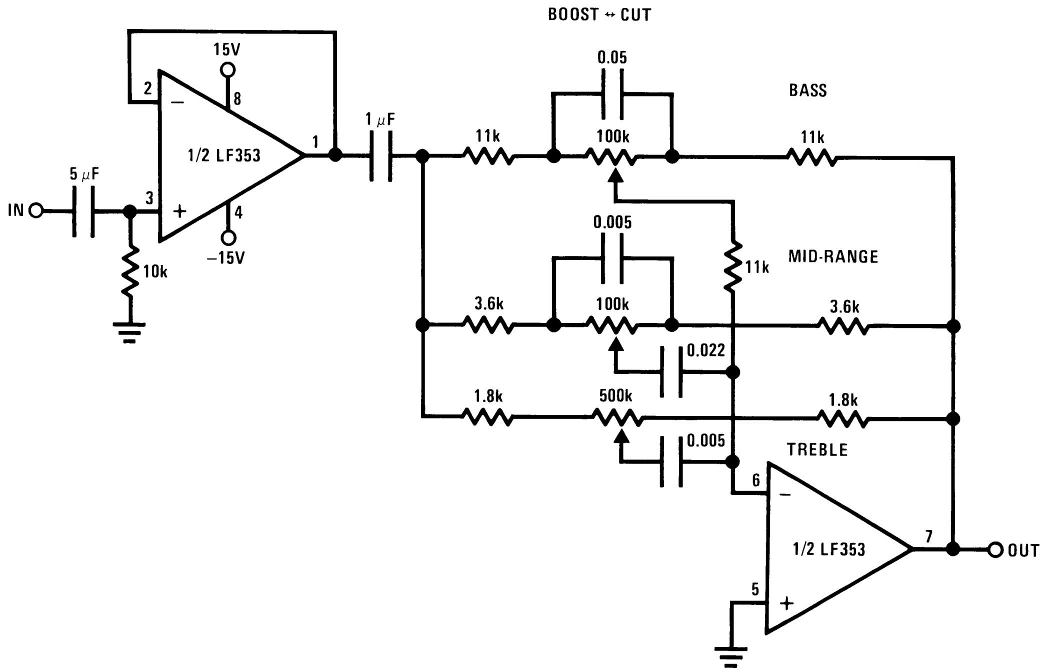
Detailed Schematic



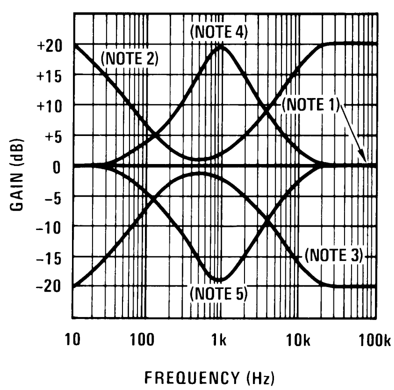
00564909

Typical Applications

Three-Band Active Tone Control



00564939



00564940

Note 1: All controls flat.

Note 2: Bass and treble boost, mid flat.

Note 3: Bass and treble cut, mid flat.

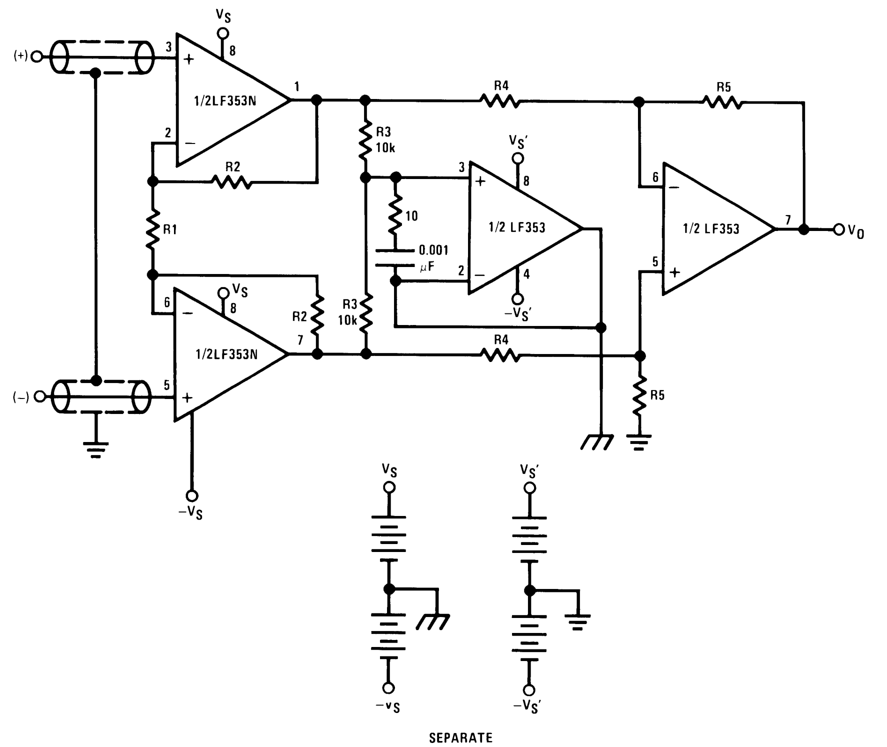
Note 4: Mid boost, bass and treble flat.

Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



00564941

$$A_V = \left(\frac{2R2}{R1} + 1\right)\frac{R5}{R4}$$

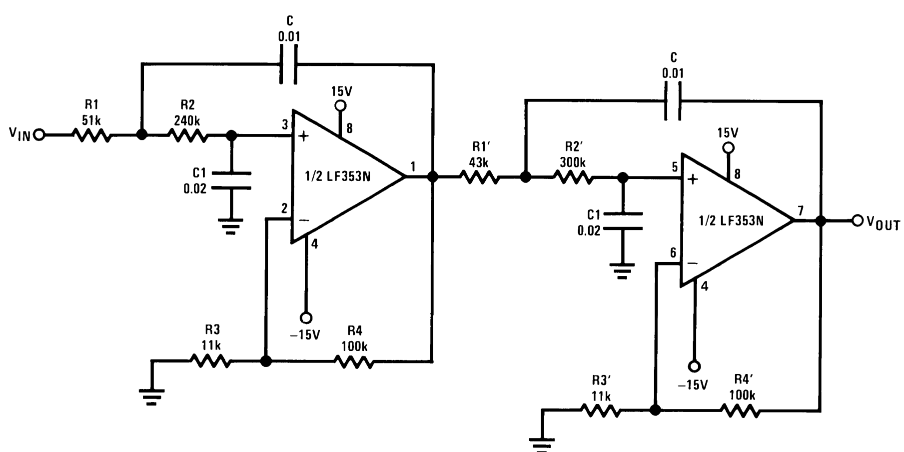
and are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{VT} = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

Fourth Order Low Pass Butterworth Filter

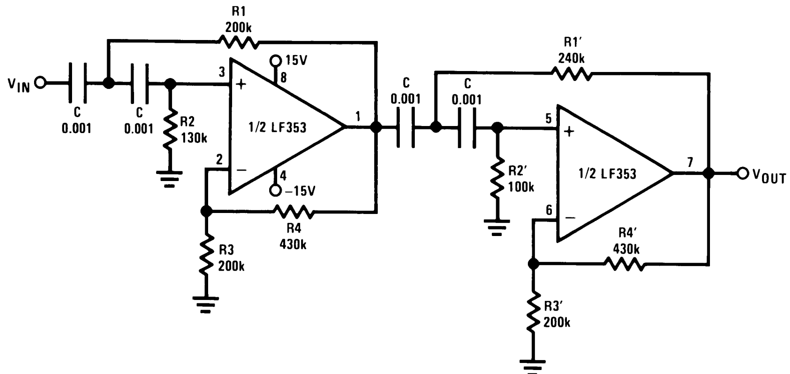


00564942

Typical Applications (Continued)

- Corner frequency (f_C) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4′/R3′)
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

Fourth Order High Pass Butterworth Filter



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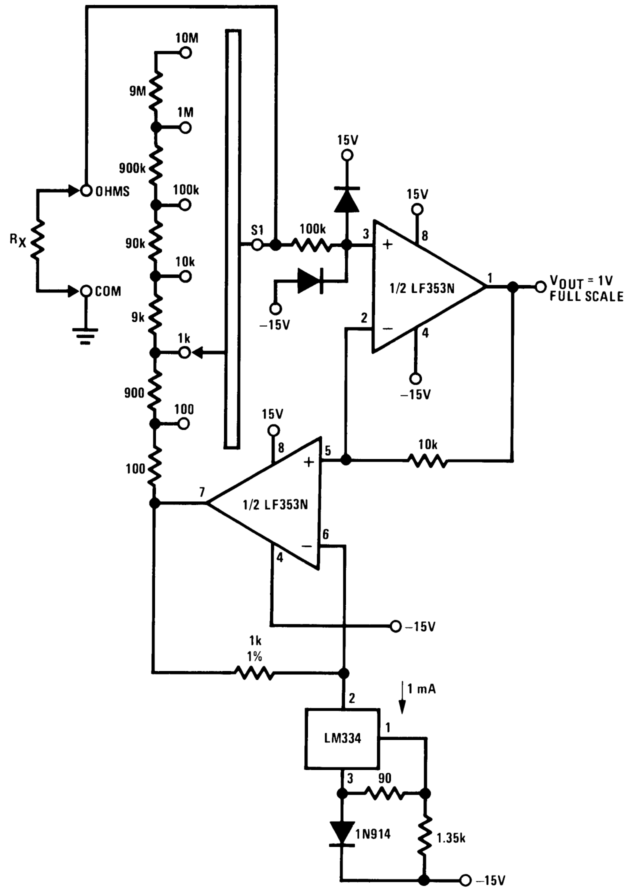
- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2C^2}} \bullet \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \bullet \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4′/R3′)
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10.

Typical Applications (Continued)

Ohms to Volts Converter

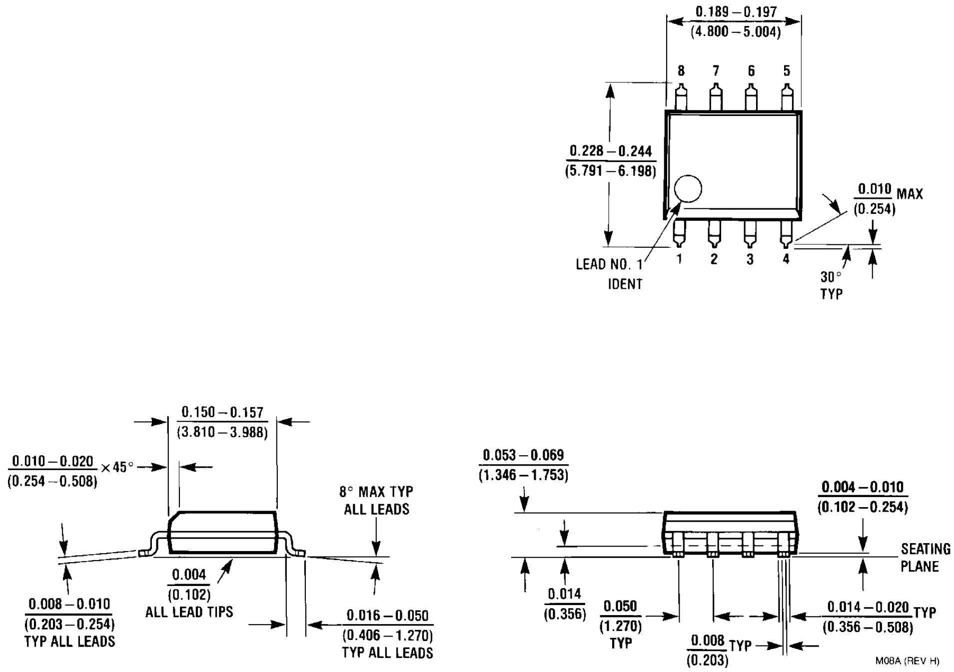


00564944

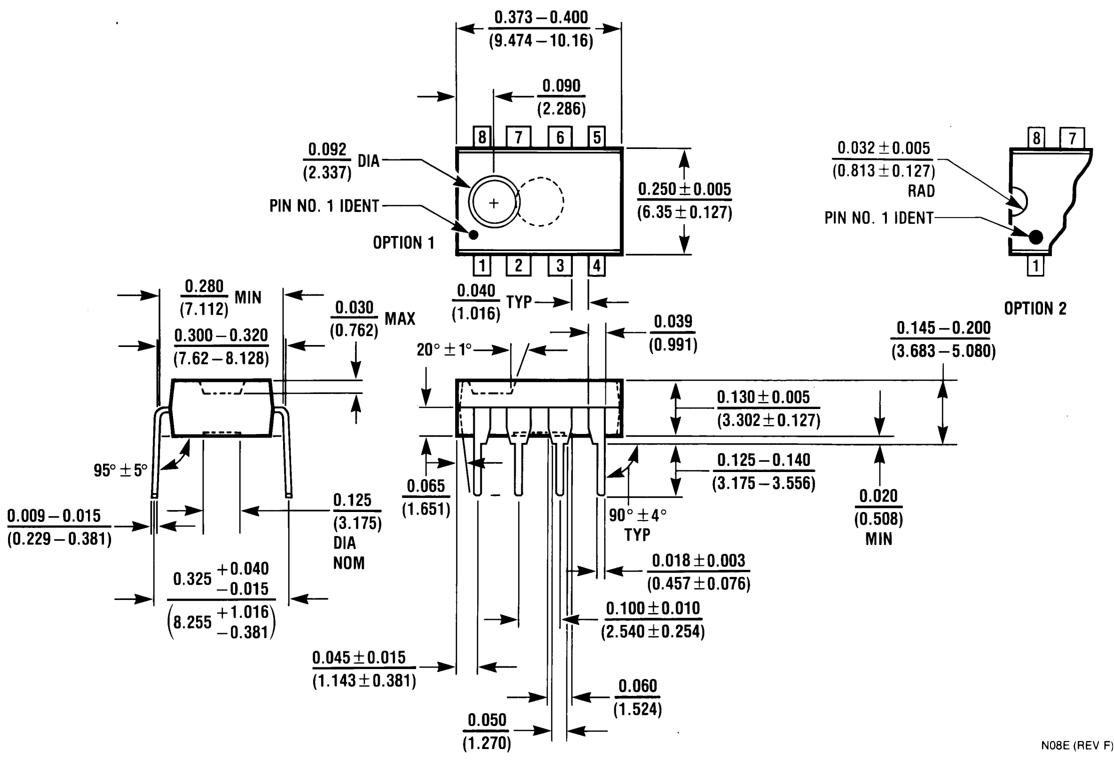
$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the LF353.

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number LF353M or LF353MX
NS Package Number M08A



Molded Dual-In-Line Package
Order Number LF353N
NS Package N08E

Notes

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